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NEUROMORPHIC PROCESSORS: DESIGN PRINCIPLES AND COMPARATIVE REVIEW

Background. The paper addresses the scientific and practical problem of designing neuromorphic processors and systems based on spiking neural networks (SNNs). Neuromorphic processors constitute a distinct class of computing systems whose operation is inspired by the biological and physical principles of the human brain. Unlike traditional von Neumann architectures, these processors integrate memory and computation, enabling massive parallelism and energy-efficient execution of complex cognitive tasks. Their hardware architecture is fundamentally based on neurons and synapses rather than transistors.

Methods. The study applies analytical and comparative methods to examine neuromorphic computing systems. Spiking neuron models are comparatively analyzed with respect to their application domains, with detailed consideration of the Integrate-and-Fire model and its mathematical formulation. Learning methods for SNNs are also evaluated, focusing on weight update mechanisms, energy efficiency, and computational complexity. Special attention is given to Spike-Timing-Dependent Plasticity (STDP). In addition, the deployment of SNNs on neuromorphic chips is analyzed, including core partitioning, routing optimization, weight storage, and learning support.

Results. The analysis identifies the advantages and limitations of spiking neuron models and learning methods for neuromorphic hardware. The Integrate-and-Fire model is shown to be the most practical engineering solution due to its simplicity and biological relevance. STDP is confirmed as an effective learning mechanism that supports adaptive behavior and energy efficiency. Architectural design choices are shown to be critical for scalable and efficient system deployment.

Conclusions. The paper presents a comparative overview of modern neuromorphic processors, emphasizing architecture, energy efficiency, and application areas. The results demonstrate the potential of neuromorphic computing for implementing SNNs and solving complex cognitive tasks. The article serves as a concise review and reference for further research in neuromorphic engineering.

Keywords: neuromorphic processor, neuromorphic architecture, spiking neural network.

Background

Every modern computer, tablet, or smartphone contains a processor – a universal device designed to execute programs. The core components of a processor's architecture include the arithmetic logic unit (ALU), memory registers, control unit, cache memory, and buses. At the heart of both central and graphics processing units are transistors – electronic switches used to transmit binary signals.

The fundamental principles behind traditional processors were established as far back as the 1940s and have changed relatively little since. The classic model of computer architecture is the von Neumann architecture – a design paradigm for a universal computing machine in which both instructions and data are stored in the same memory as binary code. The processor sequentially fetches instructions and data from memory, processes them, and carries out tasks accordingly.

For a long time, processors could only perform one operation per clock cycle. However, during the 1970s and 1980s, a technological breakthrough occurred: operating systems for personal computers began to support multitasking. The ability to run multiple programs concurrently on a single processor was achieved through resource sharing – several cycles or clock ticks were allocated to one program, then handed off to the next, and so on.

This concept of multitasking significantly influenced processor development. By the 1990s, the first multi-core processors emerged, capable of handling multiple data streams in parallel and distributing resources more efficiently. Further performance gains came from reducing transistor sizes, which allowed more of them to fit onto a single chip, boosting both processing speed and energy efficiency.

As transistor miniaturization approached physical limits in the early 2000s, silicon-based processors faced a major challenge: the material was nearing its technological boundaries. Transitioning to manufacturing processes below 5 nanometers introduced issues such as current leakage, quantum effects, and increased heat generation. These problems spurred the search for new materials and architectures – including three-dimensional structures, carbon nanotubes, and entirely new paradigms like quantum and neuromorphic computing.

Problem's Formulation. One promising direction in the pursuit of greater processor performance is the development of neuromorphic processors (NPs) – specialized chips whose operation is based on the biological and physical principles of the human brain. The field dedicated to replicating, at least partially, the brain's structure in the form of electronic circuits is known as *neuromorphic engineering* (Schuman et al., 2022). This discipline is closely tied to branches of medicine that study the anatomy and function of the biological brain, as modeling how the brain works could lead to artificial systems that mirror its structure and improve the performance of artificial intelligence systems.

Analysis of recent research and publications. The very term *neuromorphic* implies the creation of intelligent, autonomous, and asynchronous systems. The phrase *neuromorphic computing* was first introduced in the 1980s by Carver Mead, a professor at the California Institute of Technology. Mead proposed the use of analog circuits to emulate the behavior of neurons and synapses in the brain (Xiao et al., 2024). In 1989, he published the book *Analog VLSI and Neural Systems*, in which he outlined concepts for building computational systems based on biological neural networks.

The concept of neuromorphic processors is closely intertwined with the theory of neural networks and the field of neurobiology. The idea of creating artificial neural networks began to take shape in the 1940s and 1950s, when researchers became interested in designing machines capable of imitating the functions of the human brain. In 1943, Warren McCulloch and Walter Pitts proposed a mathematical model of an artificial neuron, demonstrating that a network of such neurons could perform numerical and logical operations (Mehonic et al., 2024). By the late 1950s, Frank Rosenblatt introduced an electronic device known as the *perceptron*, which is widely regarded as the first practical implementation of a neural network.

Since then, interest in neural networks has grown significantly. However, their effective implementation required alternative computational architectures – ones better suited for processing large volumes of data and unstructured information. This need gave rise to the idea of designing a new type of processor architecture that would replicate the structure of the human brain, in which information is transmitted via neurons – miniature processing elements interconnected by a vast network of signal pathways called synapses. This concept formed the basis for *spiking neural networks* (SNNs) (Spectra, n.d.).

Issues related to the optimization of SNNs and their effective deployment in neuromorphic architectures have been widely explored in scientific and applied research – see, for example, (Li, Ma, & Endoh, 2023; Liu et al., 2022). The question of implementing SNNs directly on hardware chips, addressed in works such as (Thakur et al., 2018; Ma et al., 2024), remains a key scientific and engineering challenge, as it largely determines the performance and viability of neuromorphic systems.

Starting in the 1990s, the theoretical foundations of neuromorphic engineering began to materialize in physical systems capable of mimicking the architecture and functionality of the human brain – processing data in a parallel and asynchronous manner. In 1992, S. Chip and D. M. Hotelling developed the first prototype of a circuit that emulated a biological neural system. In 1997, Hugo de Garis and his team at ATR Laboratories in Japan launched the CAM-Brain Machine project, aimed at building a large array of "neural cubes" designed to simulate an artificial brain.

Subsequent work by researchers such as K. Boahen, J. Schemmel, K. Meier, D. Modha, S. Furber, S. Al Abdul Wahid, D. Ma, A. van Schaik, G. Tang (Tang et al., 2023) and M. Ogbodo (Ogbodo et al., 2020) has been devoted to the development and practical implementation of neuromorphic chips and systems. Major tech companies, including Intel and IBM, have created commercial products based on neuromorphic engineering technologies – such as Loihi and TrueNorth, respectively. Amazon researchers are also working on the development of an AI chip incorporating neuromorphic principles.

The growing body of scientific literature devoted to the design and implementation of neuromorphic processors and systems – along with both commercial and non-commercial applications of these technologies – provides compelling evidence that neuromorphic engineering is a highly relevant and evolving field. It sits at the intersection of artificial intelligence, biology, and neurophysics, and continues to demand further research and development.

Formulation of the study purpose. The aim of this study is to analyze the current state of research on the development of neuromorphic processors and systems, and to identify the fundamental principles underlying their design and operation.

Methods

The objectives of the study include a comparative analysis of existing neuromorphic processors and systems, as well as an examination of the role and application principles of spiking neural networks (SNNs) within neuromorphic architectures. The authors do not claim scientific novelty, as the article is of a review nature and is intended to systematize and generalize existing research results in the field.

Results

A neuromorphic processor is a specialized type of processor whose architecture closely mimics the structure of biological neural networks and is specifically designed to optimize the computation of SNNs (Schumanet al., 2022). Neuromorphic processors represent a significant advancement in computational technology. By emulating the architecture of the brain, these processors aim to provide energy-efficient real-time data processing for specialized applications. The ultimate goal of neuromorphic processor architecture is to enable parallel information processing while maintaining power consumption within the range of just a few tens of watts. To achieve this, memory and processing units are integrated into a unified system – a concept known as in-memory computing.

Unlike conventional processors, the fundamental elements of a neuromorphic processor are not transistors, but rather neurons and synapses. Artificial neurons and synapses carry out computations by emulating the way biological neurons transmit signals in the brain (Mehonic et al., 2024). Each artificial neuron receives input from numerous other neurons via synapses, just as in biological neural networks. The signals transmitted through these synapses represent numerical values or weights, and the neuromorphic processor uses these weights to distribute computational load across a large number of parallel cores. These signals are activated upon reaching a specific threshold – analogous to electrical impulses in biological systems (Liu et al., 2022). This approach enables parallel data processing in a manner similar to that of the human brain. The greater the synaptic weight, the stronger the influence of the corresponding neuron on the overall computation result.

The functional diagram of a neuromorphic processor is shown in Fig. 1.

Unlike traditional CPUs and GPUs, neuromorphic chips are characterized by the following key components:

1. Neural cores – hardware blocks designed to model the behavior of neurons and synapses. A single neural core simulates multiple spiking neurons and manages their interconnections.
2. Event-driven communication – connections between neurons that operate based on event-triggered signaling rather than continuous data flow.
3. Local memory – used to store synaptic weights, with the primary goal of reducing energy consumption associated with data transfers.
4. Plasticity mechanisms – designed to enable learning within the internal neural network by adapting synaptic weights over time.

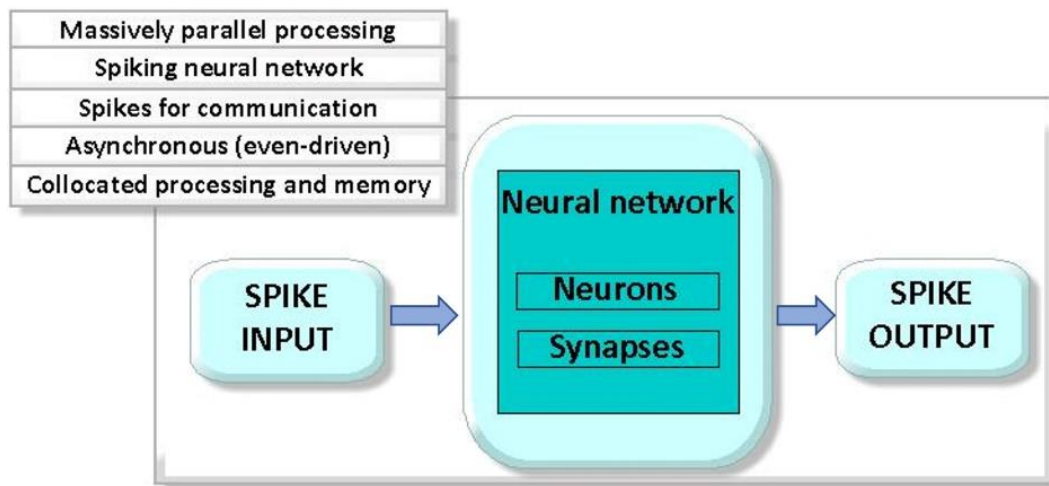


Fig. 1. Neuromorphic processor

Neuromorphic processors emulate the functioning of the human brain by breaking down complex computational tasks into simpler operations, which are then parallelized and processed simultaneously (Xiao et al., 2024). Neuromorphic computing differs from classical approaches – such as those based on convolutional neural networks (CNNs) – in that it more accurately mimics the brain through the use of SNNs. These networks simulate the behavior of biological neurons by taking into account the temporal dynamics of signal transmission (Fig. 2).

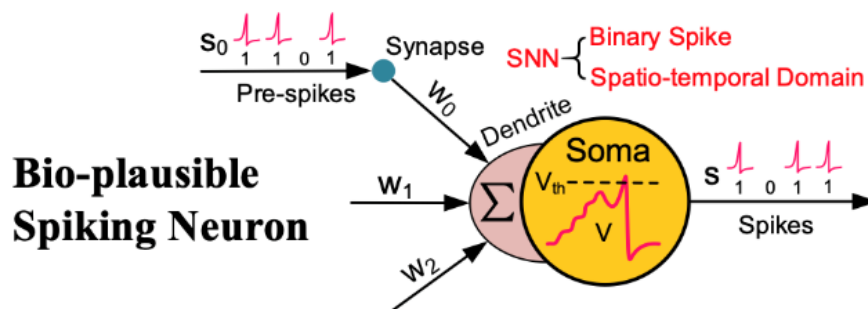


Fig. 2. SNN architecture (Spectra, n.d.)

The Spiking Neural Network (SNN) is the foundational element of a neuromorphic processor. SNNs emerged in the late 1990s and are considered the third generation of artificial neural networks. Unlike first- and second-generation networks, neurons in SNNs communicate using discrete spikes of uniform amplitude. Neuromorphic processors employ SNNs to emulate brain function at a level that is more biologically realistic than that offered by traditional artificial neural networks (Rose et al., 2021).

The key distinction between SNNs and conventional neural networks lies in how information is transmitted. In SNNs, data is not communicated through continuous signals, but rather through discrete events – brief bursts of activity known as spikes. A neuron emits a spike only after it has accumulated sufficient input to exceed an internal threshold. In other words, neurons do not operate continuously, which forms the basis for the energy efficiency of such systems.

These neural structures support a high degree of parallelism in spike propagation. Unlike traditional networks where inputs and outputs are numeric vectors, SNNs use temporal sequences of discrete events (spikes) as both input and output. This event-driven representation enables asynchronous computation, activating only those parts of the network directly involved in processing a given event (Ahmed, & Shereif, 2022).

To implement spiking neurons within the neural cores of neuromorphic processors, four primary models are commonly used (Al Abdul Wahid, Asad, & Mohammadi, 2024):

- the Hodgkin-Huxley model;
- the Izhikevich model;
- the Integrate-and-Fire model;
- the Spike Response model (Hendy, & Merkel, 2022).

A comparative overview of these spiking neuron models is provided in Table 1.

As shown in Table 1, the Leaky Integrate-and-Fire (LIF) model is the simplest and fastest among the spiking neuron models (Hendy, & Merkel, 2022). For this reason, it is widely used in engineering applications, despite lacking biological mechanisms for neuron adaptation and realistic spike patterns.

Table 1

Comparative characteristics of spiking neuron models				
	Hodgkin-Huxley model	Izhikevich model	Integrated-and-Fire model	Spike Response model
Mathematical basis	Equations describing the dynamics of ion channels in the neuron membrane	An empirical description of neural dynamics	Description of the dynamics of the membrane potential	Convolution of input pulses with response kernels
Biological accuracy	High	Average	Low	Average
Computational complexity	High	Average	Low	Average
Application field	Biology, neurophysiology	Neuromorphic systems, big SNN	Neuroengineering, computing SNN	Theoretical modeling, SNN

The mathematical foundation of an SNN based on the LIF model is composed of equations that describe the dynamics of a neuron's membrane potential and the mechanisms of synaptic transmission. The membrane potential dynamics can be expressed as:

$$\tau_m \frac{dV(t)}{dt} = -(V(t) - V_r) + RI(t), \quad (1)$$

where τ_m – membrane time constant, $V(t)$ – membrane potential, V_r – resting potential, R – membrane resistance, $I(t)$ – input current.

When $V(t)$ reaches a certain threshold, the neuron emits a spike, and the membrane potential is reset to V_r .

Synaptic transmission is characterized by the synaptic current, which can be modeled using an exponential decay function:

$$\tau_s \frac{dI_s(t)}{dt} = -I_s(t) + \sum_k \omega_k \delta(t - t_k), \quad (2)$$

where τ_s – synaptic time constant, ω_k – weight of the k -th synapse, t_k – time of spike arrival, $\delta(t - t_k)$ – delta function modeling the instantaneous arrival of a spike.

The algorithm for updating synaptic weights in an SNN depends on the selected learning rule used to train the neural network. The most commonly employed learning paradigms – including those applicable to SNNs – are as follows (Al Abdal Wahid, Asad, & Mohammadi, 2024):

1. Unsupervised Learning – in this approach, the neural network identifies patterns in the data without labeled inputs. For SNNs, common methods include Spike-Timing-Dependent Plasticity (STDP), Homeostatic Plasticity, and genetic algorithms. These methods are considered the most biologically plausible and feature low computational complexity, making them particularly suitable for neuromorphic processors. They are typically executed locally on-chip, without the need for external computing resources.

2. Supervised Learning – this method requires labeled data for training. In the context of SNNs, techniques such as Spike-Prop and Surrogate Gradient Descent are employed. While these methods offer moderate computational complexity, they are less biologically realistic and are generally executed externally on a CPU or GPU. They are most commonly used in training deep or hybrid SNNs, and in broader applications of machine learning and GPU-accelerated training.

3. Reinforcement Learning (RL) – this paradigm trains neural networks using a reward system for correct actions. Examples of RL methods for SNNs include Voltage-Dependent STDP, Q-learning, and Deep Q-Networks. These methods are computationally intensive, biologically less plausible, and typically executed in a hybrid mode, with some components running on the chip and others offloaded to a CPU. Key application areas include autonomous agents, and solving discrete or complex reinforcement learning tasks.

Spike-Timing-Dependent Plasticity (STDP) is the most widely used learning method for SNNs implemented in neuromorphic processor architectures (Zhang, Gu, & Pan, 2018). In STDP, the synaptic weight update $\Delta\omega$ depends on the time difference Δt between the arrival of the presynaptic spike (t_{pre}) and the postsynaptic spike (t_{post}). Mathematically, the STDP rule can be expressed as:

$$\begin{aligned} \Delta\omega &= A_+ e^{-\Delta t / \tau_+}, \text{ if } \Delta t > 0, \\ \Delta\omega &= -A_- e^{-\Delta t / \tau_-}, \text{ if } \Delta t < 0, \end{aligned} \quad (3)$$

where A_+ , A_- – plasticity coefficients, τ_+ , τ_- – time constants.

If the presynaptic spike arrives before the postsynaptic spike ($\Delta t > 0$), the synapse is strengthened. Conversely, if the presynaptic spike arrives after the postsynaptic spike ($\Delta t < 0$), the synapse is weakened. To prevent unbounded weight growth, a constraint is typically applied, which can be described by the following expression:

$$\omega = \max(\omega_{\min}, \min(\omega_{\max}, \omega + \Delta\omega)), \quad (4)$$

where $\omega_{\min}$, $\omega_{\max}$ – the minimum and maximum allowable synaptic weights, respectively.

In theory, SNNs consume less energy and operate faster than second-generation artificial neural networks. Some key advantages of SNNs over both first- and second-generation networks include:

- Efficient modeling of temporal, spatiotemporal, or spectrotemporal data;
- Support for multiscale temporal processing;
- Linking higher-level functional behavior with lower-level genetic mechanisms;
- Integration of multiple modalities – such as audio and visual data – within a single system;

- Predictive modeling and event forecasting;
- High-speed, massively parallel information processing;
- Compact data representation and computation;
- Scalable architectures, from tens to billions of spiking neurons;
- Low power consumption, especially when implemented on neuromorphic hardware.

The process of deploying an SNN onto a neuromorphic processor chip involves partitioning the network across neural cores, optimizing signal routing, storing synaptic weights, and supporting the learning process (Zhang, Gu, & Pan, 2018), as illustrated in Fig. 3.

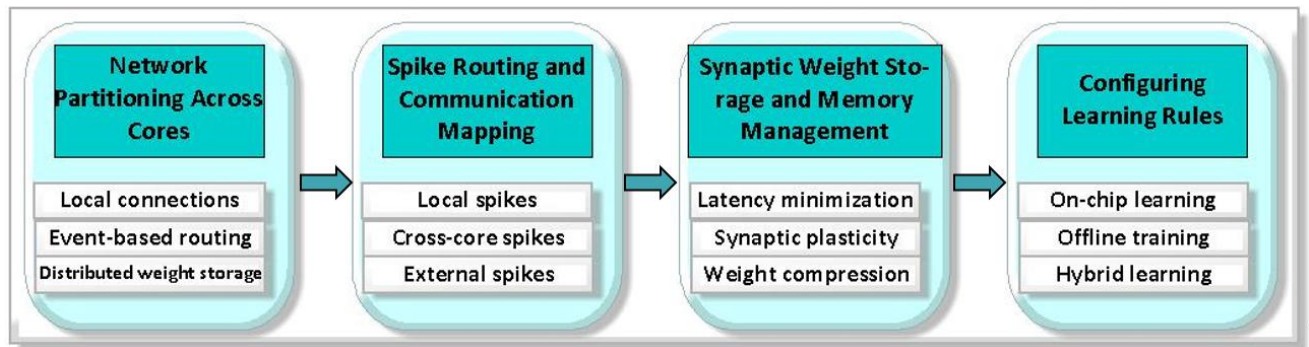


Fig. 3. Key steps for deploying an SNN on a neuromorphic processor chip

The use of spiking neural networks (SNNs) endows neuromorphic processors with the following distinctive characteristics:

1. Integration of memory and computation. In traditional computers, data must be transferred between memory and the processor for computations to occur, creating bottlenecks. Neuromorphic chips integrate memory and computational elements, minimizing latency and reducing power consumption.

2. Asynchronous operation. Unlike conventional processors, which operate at a fixed clock frequency, neuromorphic chips can function asynchronously – activating only when needed to process information. This significantly improves energy efficiency.

3. Event-driven processing. Neuromorphic processors process data using an event-based model, meaning they are triggered only when a specific event occurs. This mirrors the behavior of biological neurons, which "fire" only when a certain threshold is reached.

4. Parallel processing. Much like the human brain, neuromorphic processors are designed for massively parallel computation, enabling them to process large volumes of information simultaneously. This makes them particularly effective in tasks such as pattern recognition and audio analysis.

5. Plasticity. Certain neuromorphic systems are capable of learning and adaptation by modifying the connections between neurons – a phenomenon known as synaptic plasticity. This enables such systems to be flexible and capable of self-learning.

The principles of neuromorphic engineering have inspired the development of both commercial and academic projects focused on the design and implementation of neuromorphic chips, processors, and systems. Rather than performing arithmetic operations in a sequential or parallel fashion like conventional CPUs or GPUs, neuromorphic processors are designed to replicate the structure and functional principles of the human brain.

A comparative overview of early neuromorphic processors and systems is presented in Table 2.

In addition to individual neuromorphic processors described in Table 2, researchers and developers in the field of neuroengineering have announced the creation of neuromorphic supercomputers based on these processors.

In December 2023, researchers from Western Sydney University, Australia, reported the development of the world's first neuromorphic supercomputer capable of performing approximately 228 trillion synaptic operations per second – a level of performance comparable to that of the human brain. The neuromorphic machine, named DeepSouth, is expected to process vast volumes of data at high speed while consuming significantly less energy than conventional supercomputers.

In 2024, Intel announced the release of the world's largest neuromorphic computing system, known as HalaPoint. This system, housed at Sandia National Laboratories in New Mexico, USA, is designed to emulate brain-like information processing. Its neuronal capacity is roughly equivalent to that of an owl or a small monkey. A key advantage of this architecture is its extremely low power consumption during idle states, unlike conventional GPUs, which maintain relatively high energy usage even when not actively computing.

A comparative overview of the latest neuromorphic systems, DeepSouth and HalaPoint, is presented in Table 3.

At present, neither DeepSouth nor HalaPoint provides unrestricted open access for independent experimental research. DeepSouth use is currently limited to internal projects and institutional collaborations. HalaPoint is similarly not publicly accessible; however, research groups may obtain controlled access through participation in the Intel Neuromorphic Research Community or through formal research partnerships. Thus, experimental studies on these platforms are generally conducted within collaborative or invitation-based frameworks rather than through open-access infrastructure. When comparing the performance of the neuromorphic systems DeepSouth and HalaPoint, it becomes evident that their developers have approached data processing speeds comparable to those of the human brain. However, the cognitive capabilities of these systems – even the most advanced – still fall significantly short of the human brain's potential. Neuromorphic systems have yet to achieve the level of adaptability, flexibility, and neuroplasticity that is inherent to biological neural networks.

Table 2**Comparative Overview of Key Features of Neuromorphic Processors and Early Neuromorphic Systems**

	Neurogrid	BrainScaleS	TrueNorth	SpiNNaker	Loihi2
Technology	Analog	Analog	Digital	Digital	Digital
Year of creation	2009	2011	2014	2018	2018
Creator	Stanford University, USA. Kwaben Boahen	University of Heidelberg, Germany. Johannes Schemmel, Karlheinz Meier	IBM company, USA. Dharmendra Modha	University of Manchester, UK. Steve Furber	Intel Labs Neuromorphic Computing Research Group, USA.
Chip size	1,7 cm ²	0,5 cm ²	4,3 cm ²	1 cm ²	31 mm ²
Neurons	1 million	200,000	1 million	768,000	1 million
Synapses	4 billion	40 million	256 million	768 million	120 million
Power efficiency	5 W	500 W	70 mW	80 W	From a few milliwatts to several watts, depending on the task
Information processing	Exact value undisclosed	Operates ~10,000× faster than biological neurons.	46 billion synaptic operations per second	Up to 1 quadrillion synaptic updates per second	Up to 1 million events (spikes) per second per core
Scope of application	Neural modeling and visualization experiments	Neuroscience studies, robotics control, AI acceleration, cognitive computing	Pattern recognition, sensor data processing	Brain simulation, AI, and robotics	Adaptive AI, brain-like decision-making, power-efficient AI, scientific Computing

Table 3**Comparative Overview of the Latest Neuromorphic Systems**

	DeepSouth	HalaPoint
Technology	Digital	Digital
Neurons	billions	Up to 1,15 billion
Synapses	trillions	128 billion
Neural core	-	1152 Loihi2 chips and 2300 additional processors based on x86 architecture
Information processing	Event-driven, parallel, programmable	Event-driven, parallel, programmable
Power efficiency	Not disclosed	2600 W
Dimensions	Not disclosed	6U chassis
Learning	1. STDP 2. RL	Programmable learning rules of the Loihi2 processor
Processing speed	228 ¹² synaptic operations per second	380 ¹² synaptic operations/sec, 240 ¹² neuronal operations/sec, up to 20 ¹⁵ other operations/sec
Cognitive abilities	Pattern recognition, sensory processing, decision-making, adaptive learning	Real-time pattern recognition, decision-making, and brain-like neuroplastic mechanisms

Discussion and conclusions

This study presents an integrated analytical and comparative overview of modern neuromorphic processors and systems, which represent a fundamentally different, non-von Neumann approach to computing, grounded in biophysical principles and the use of spiking neural networks (SNNs). Neuromorphic architectures tightly couple memory and computation, thereby eliminating traditional data transfer bottlenecks and enabling more efficient execution of complex cognitive and perception-oriented tasks compared to conventional CPU- and GPU-based artificial intelligence systems. Mathematical modeling of SNNs provides a balanced compromise between biological plausibility and computational efficiency, which is one of the key reasons developers of neuromorphic systems report significant advantages in performance and energy consumption.

A defining feature of neuromorphic systems is their event-driven nature: artificial neurons activate only in response to relevant stimuli rather than processing data continuously. This operational paradigm leads to substantial reductions in energy usage and makes neuromorphic processors particularly attractive for specialized applications such as pattern recognition, sensor data processing, autonomous vehicle control, and audio and video analysis. In these narrow AI domains, neuromorphic systems already demonstrate high efficiency and practical relevance, and their adoption continues to grow.

At the same time, this paper provides a comprehensive analytical review and systematic comparison of existing neuromorphic processors, architectures, spiking neuron models, and learning mechanisms. Particular attention is given to

current trends in neuromorphic computing, including the increasing scale of neuromorphic platforms, the predominance of event-driven architectures, and the widespread use of simplified neuron models, such as Leaky Integrate-and-Fire, in real-world implementations. This comparative synthesis allows the identification of key design principles, architectural trade-offs, and performance characteristics that shape contemporary neuromorphic systems.

Despite notable progress toward achieving brain-level processing speeds and superior energy efficiency, neuromorphic engineering introduces a number of significant challenges. The radical departure from the von Neumann paradigm necessitates a reassessment of established approaches in both hardware and software design. The effective exploitation of neuromorphic architectures will require the development of new programming models and languages, as well as next-generation memory technologies, data storage solutions, sensors, and revised principles of hardware integration. In addition, the analysis reveals several persistent research gaps, particularly in cognitive flexibility, scalable on-chip learning, and the limited accessibility of large-scale neuromorphic platforms for independent experimental research.

Finally, although neuromorphic systems offer theoretical and practical advantages for solving specific computational problems, they still cannot rival the human brain in tasks that require abstract reasoning, deep analysis, and general intelligence. Human cognition is characterized by tightly interconnected capabilities, enabling adaptability, transfer of knowledge, and sophisticated problem-solving in novel situations. Existing neuromorphic systems remain limited in terms of neuroplasticity, adaptability, and general cognitive competence. Nevertheless, by synthesizing current research and identifying open challenges, this study provides an integrated analytical perspective that may support future research directions and the development of more flexible, scalable, and biologically inspired neuromorphic systems.

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Use of Artificial Intelligence. The authors declare that no generative artificial intelligence tools or other AI technologies were used in the preparation of this manuscript, data analysis, and writing of the text. The work is a completely original product of the authors' intellectual activity.

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НЕЙРОМОРФНІ ПРОЦЕСОРИ: ПРИНЦИПИ ПРОЕКТУВАННЯ ТА ПОРІВНЯЛЬНИЙ ОГЛЯД

Вступ. У статті розглядається науково-практична проблема проектування нейроморфних процесорів і систем на основі імпульсних нейронних мереж (SNN). Нейроморфні процесори становлять окремий клас обчислювальних систем, робота яких натхненна біологічними та фізичними принципами функціонування людського мозку. На відміну від традиційних архітектур фон Неймана, ці процесори інтегрують пам'ять і обчислення, забезпечуючи масовий паралелізм і енергоефективне виконання складних когнітивних завдань. Їх апаратна архітектура базується на нейронах і синапсах, а не на транзисторах.

Методи. У дослідженні застосовуються аналітичні та порівняльні методи для вивчення нейроморфних обчислювальних систем. Моделі імпульсних нейронів порівнюються за сферами застосування з детальним розглядом моделі «Інтегруй і стріляй» та її математичної формулювання. Також оцінюються методи навчання для SNN, з акцентом на механізмах оновлення ваги, енергоефективності та обчислювальній складності. Особлива увага приділяється Spike-Timing-Dependent Plasticity (STDP). Крім того, аналізується розгортання SNN на нейроморфних чіпах, включаючи розподіл ядер, оптимізацію маршрутизації, зберігання ваги та підтримку навчання.

Результати. Аналіз визначає переваги та обмеження моделей спайкових нейронів та методів навчання для нейроморфного обладнання. Модель «Інтегруй та стріляй» виявилася найбільш практичним інженерним рішенням завдяки своїй простоті та біологічній релевантності. STDP підтвердилася як ефективний механізм навчання, що підтримує адаптивну поведінку та енергоефективність. Вибір архітектурного дизайну виявився критично важливим для масштабованого та ефективного розгортання системи.

Висновки. У статті представлено порівняльний огляд сучасних нейроморфних процесорів з акцентом на архітектуру, енергоефективність та області застосування. Результати демонструють потенціал нейроморфних обчислень для реалізації SNN та вирішення складних когнітивних завдань. Стаття слугує стислим оглядом та довідником для подальших досліджень у галузі нейроморфної інженерії.

Ключові слова: Нейроморфний процесор, нейроморфна архітектура, спайкова нейронна мережа

Автори заявляють про відсутність конфлікту інтересів. Спонсори не брали участі в розробленні дослідження; у зборі, аналізі чи інтерпретації даних; у написанні рукопису; в рішенні про публікацію результатів.

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